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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SCHWABE, WILLIAMSON & WYATT, P.C.
PACWEST CENTER, SUITE 1900
1211 SW FIFTH AVENUE
PORTLAND, OR 97204

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 08/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,562	BOATRIGHT ET AL.	
	Examiner	Art Unit	
	Michael C. Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9,12,14-19,21 and 23-30* is/are rejected.

7)☒ Claim(s) *8,10,11,13,20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/1/04; 8/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the dynamic random access memory in claims 25 and 28 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 25 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not disclose a dynamic random access memory coupled to an integrated circuit.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 4-7, 9, 12, 14, 16, 18, 19, 21, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Fields, Jr. et al., US 2003/0145257 A1.

Referring to claim 1:

a. In paragraph 0028, Fields, Jr. et al. disclose that when a new error is detected it is assumed to be a soft error and the corresponding address of the

error is saved (detecting a first location-independent error within an area of a cache memory).

b. In paragraph 0038, Fields, Jr. et al. disclose comparing the current address of the error with a previously saved address of another error to determine it is the second occurrence of a single bit error (determining whether the first error is a second consecutive error associated with the area).

c. In paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (and preventing further use of the area if the error is determined to be the second consecutive error associated with the area).

Referring to claim 4, in paragraph 0030, Fields, Jr. et al. disclose that when the process receives a bit error which turns out to be a hard error, it again checks for the source of the bit error. Then, it detects that an address is previously saved in the storage indicating that this is not a first time error. Next, it compares the error address to the previously saved address (comparing a current operation address corresponding to the first error with a stored address corresponding to a previous error). The process detects a hard error if the compared addresses are the same (and identifying the first error as the second consecutive error if the current operation address matches the stored address).

Referring to claim 5, in paragraph 0029, Fields, Jr. et al. disclose comparing the error address to the previously saved address. A soft error is further detected if the addresses are not the same when compared. The address of this later bit error is then

saved ready for another comparison when the next error occurs (storing the current operation address corresponding to the first error in place of the stored address corresponding to the previous error if the current operation address does not match the stored address).

Referring to claim 6, in paragraph 0030, Fields, Jr. et al. disclose that the process detects a hard error if the compared addresses are the same (accessing the current operation address corresponding to the first error a second time to determine whether the second consecutive error occurs).

Referring to claim 7, in paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (wherein the area comprises a cache line and wherein preventing further use of the area further comprises: selecting the cache line; and modifying a cache management system to at least inhibit subsequent access to the selected cache line).

Referring to claims 9, 14, and 23, in paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (wherein modifying a cache management system comprises assigning a disable state to the cache line).

Referring to claim 12:

a. In paragraph 0028, Fields, Jr. et al. disclose that when a new error is detected it is assumed to be a soft error and the corresponding address of the error is saved (detecting a first error within a cache line of a cache memory).

b. In paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (disabling the cache line of the cache memory; and dynamically modifying a cache management system to at least inhibit subsequent access to the disabled cache line by a processor).

Referring to claim 16:

a. In paragraph 0024, Fields, Jr. et al. disclose a cache memory.

b. In paragraph 0028, Fields, Jr. et al. disclose that when a new error is detected it is assumed to be a soft error and the corresponding address of the error is saved (error detection logic coupled to the cache memory, the error detection logic equipped to detect a first location-independent error within an area of the cache memory).

c. In paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (determine whether the first error is a second consecutive error associated with the area; and prevent further use of the area if the error is determined to be the second consecutive error associated with the area).

Referring to claim 18:

a. In paragraph 0022, Fields, Jr. et al. disclose error correction code to correct single bit error (error checking and correcting logic to detect an error within the cache memory).

b. In paragraph 0030, Fields, Jr. et al. disclose detecting a hard error by comparing the error address to the previously saved address (hard error detection logic to determine whether the detected error is a hard error).

c. In paragraph 0038, Fields, Jr. et al. disclose deleting a cache line if a hard error is detected (cacheline disable logic to disable a cacheline affected by the error if it is determined that the detected error is a hard error).

Referring to claim 19:

a. In paragraph 0029, Fields, Jr. et al. disclose comparing the error address to the previously saved address. A soft error is further detected if the addresses are not the same when compared. The address of this later bit error is then saved ready for another comparison when the next error occurs (an error register to store address information indicating at least the cacheline affected by the error).

b. In paragraph 0030, Fields, Jr. et al. disclose that when the process receives a bit error which turns out to be a hard error, it again checks for the source of the bit error. Then, it detects that an address is previously saved in the storage indicating that this is not a first time error. Next, it compares the error address to the previously saved address (comparison logic to compare stored address information with a current operating address).

c. In paragraph 0030, Fields, Jr. et al. disclose that the process detects a hard error if the compared addresses are the same (state logic to determine

whether the error is a second consecutive error based upon output from the comparison logic).

Referring to claim 21:

a. In paragraph 0024, Fields, Jr. et al. disclose a cache memory.

b. In paragraph 0028, Fields, Jr. et al. disclose that when a new error is detected it is assumed to be a soft error and the corresponding address of the error is saved (error detection logic coupled to the cache memory, the error detection logic equipped to detect a first error within a cache line of a cache memory).

c. In paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (disable the cache line of the cache memory; and dynamically modify a cache management system to at least inhibit subsequent access to the disabled cache line by a processor).

6. Claims 12, 15, 21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Arimilli et al., U.S. Patent 6,006,311.

Referring to claim 12:

a. In column 3, lines 56-60, Arimilli et al. disclose that when a cache chip is fabricated, it can be tested to determine if there are any defective row or column lines in each of the arrays (detecting a first error within a cache line of a cache memory).

b. In column 3, lines 60-61, Arimilli et al. disclose that if an array is defective, a fuse can be permanently blown to indicate its defective nature (disabling the

cache line of the cache memory; and dynamically modifying a cache management system to at least inhibit subsequent access to the disabled cache line by a processor).

Referring to claim 21:

a. In column 5, lines 64-67, Arimilli et al. disclose a set associative cache (a cache memory).

b. In column 3, lines 56-60, Arimilli et al. disclose that when a cache chip is fabricated, it can be tested to determine if there are any defective row or column lines in each of the arrays (error detection logic coupled to the cache memory, the error detection logic equipped to detect a first error within a cache line of a cache memory).

c. In column 3, lines 60-61, Arimilli et al. disclose that if an array is defective, a fuse can be permanently blown to indicate its defective nature (disable the cache line of the cache memory; and dynamically modify a cache management system to at least inhibit subsequent access to the disabled cache line by a processor).

Referring to claims 15 and 24, in column 7, lines 58-61, Arimilli et al. disclose that each time the computer is booted, the mask might be automatically updated based on firmware testing, as part of the boot process (wherein the first error is detected via programmable built-in self test (PBIST) logic).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2-3, 17, and 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fields, Jr. et al., US 2003/0145257 A1.

Referring to claims 2 and 17, in paragraph 0009, Fields, Jr. et al. disclose a cache composed of cache lines, however, Fields, Jr. et al. don't explicitly disclose an n-way set associative static random access memory. The Examiner takes Official Notice that an n-way set associative static random access memory is well known. For example, it is used as router buffers and caches where speed is the prime requirement. It would have been obvious to one of ordinary skill at the time of the invention to include the n-way set associative static random access memory into the system of Fields, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because SRAM is faster than DRAM thus enabling the memory accesses to be faster and increasing processing speed.

Referrring to claim 3, in paragraph 0022, Fields, Jr. et al. dislcose that the single bit error is detected by ECC (wherein the location-independent error comprises an error checking and correcting (ECC) based error.

Referring to claim 25:

a. In Figure 1 and paragraph 0017, Fields, Jr. et al. disclose local memories attached to a processing system. However, Fields, Jr. et al. don't explicitly disclose that the local memory is a dynamic random access memory. The Examiner takes Official Notice that in the art of computer systems it is well known to have a DRAM attached to a processor and a cache. An example of this would be most computer systems. It would have been obvious to one of ordinary skill at the time of the invention to include the DRAM into the system of Fields, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because DRAM is simple circuitry that allows for a large dense memory used for temporary storage.

b. In Figure 2, Fields, Jr. et al. disclose an integrated circuit coupled to the dynamic random access memory, the integrated circuit including a cache memory and error detection logic.

d. In paragraph 0028, Fields, Jr. et al. disclose that when a new error is detected it is assumed to be a soft error and the corresponding address of the error is saved (detect a first location-independent error within an area of the cache memory).

e. In paragraph 0038, Fields, Jr. et al. disclose comparing the current address of the error with a previously saved address of another error to determine it is the second occurrence of a single bit error (determine whether the first error is a second consecutive error associated with the area).

f. In paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (and prevent further use of the area if the error is determined to be the second consecutive error associated with the area).

Referring to claims 26 and 29, in Figures 1 and 2, Fields, Jr. et al. disclose wherein the integrated circuit further includes a central processing unit and at least one input/output module coupled to the central processor unit.

Referring to claims 27 and 30, in paragraph 0017, Fields, Jr. et al. disclose that the integrated circuit is a microprocessor.

Referring to claim 28:

a. In Figure 1 and paragraph 0017, Fields, Jr. et al. disclose local memories attached to a processing system. However, Fields, Jr. et al. don't explicitly disclose that the local memory is a dynamic random access memory. The Examiner takes Official Notice that in the art of computer systems it is well known to have a DRAM attached to a processor and a cache. An example of this would be most computer systems. It would have been obvious to one of ordinary skill at the time of the invention to include the DRAM into the system of Fields, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because DRAM is simple circuitry that allows for a large dense memory used for temporary storage.

b. In Figure 2, Fields, Jr. et al. disclose an integrated circuit coupled to the dynamic random access memory, the integrated circuit including a cache memory and error detection logic.

g. In paragraph 0028, Fields, Jr. et al. disclose that when a new error is detected it is assumed to be a soft error and the corresponding address of the error is saved (detect a first error within a cache line of the cache memory).

h. In paragraph 0038, Fields, Jr. et al. disclose that if it is the second occurrence of a single bit error the cache line is deleted (disable the cache line of the cache memory; and dynamically modify a cache management system to at least inhibit subsequent access to the disabled cache line by a processor).

Allowable Subject Matter

9. Claims 8, 10, 11, 13, 20, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter.

Referring to claim 8, the prior art does not teach or reasonably suggest wherein modifying a cache management system comprises modifying a value corresponding to a particular set such that the cache line is less likely to be accessed than at least one other cache line upon one or more further cache accesses by a processor.

Referring to claim 10, the prior art does not teach or reasonably suggest wherein the disable state is assigned as part of a MESI state assignment.

Referring to claim 11, the prior art does not teach or reasonably suggest determining whether data stored in the area of cache memory has been modified as compared to data stored in a corresponding area of main memory; facilitating recovery of the modified data stored in the area of cache memory; and preventing further use of the area of the cache memory after the modified data stored in the area of cache memory has been recovered.

Referring to claim 13, the prior art does not teach or reasonably suggest wherein modifying a cache management system comprises modifying a value stored in a register corresponding to the cache line and associated with implementation of a least recently used algorithm, such that the cache line is less likely to be accessed than at least one other cache line within the cache memory upon one or more further cache accesses by a processor.

Referring to claim 20, the prior art does not teach or reasonably suggest wherein the cacheline disable logic further comprises: a decoder to generate a way-disable vector prevent further use of the area; and way-select logic to select the cacheline to be disabled based upon the way-disable vector; wherein the way-disable vector operates to modify a cache management system including at least one of a least recently used (LRU) algorithm and a MESI protocol.

Referring to claim 22, the prior art does not teach or reasonably suggest wherein the error detection logic is further equipped to modify a value stored in a register

corresponding to the cache line and associated with implementation of a least recently used algorithm, such that the cache line is less likely to be accessed than at least one other cache line within the cache memory upon one or more further cache accesses by a processor.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited prior art is related to cache error detection and correction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C. Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael C Maskulinski
Examiner
Art Unit 2113